



**Thumbs Down:** Touch to find what are the non-INDUSTRY coding practices followed in the below code. Number is updated automatically

A **Long Touch** on the editor window pops up a menu. Choose "**Create Testbench**" to create template for you. SAVES lot of CODING.

**Thumbs Up:** Touch to find what are the INDUSTRY coding practices followed in the below code. Number is updated automatically

**Syntax Errors:** Touch to find what are the Syntax ERRORS in the below code. Number is updated automatically

**About:** Release and VGuru information

**Menu:** Touch this to get the menu displayed here.

**Insert :** To insert Verilog specific symbol or operator without searching the standard keyboard.

**Wizard:** Wizard to create Verilog design or testbench template. Just enter the fields.

**Disable KeyWord :** Disables keyword lookup. If enabled, type two letters to display matching words

**File:** Opens file in the directory /VGuru/Verilog/\*.vhd. Compiles automatically and displays Recommended, non-recommended and Syntax errors.

**Disable VNext :** Disables VNext which guides automatically. Use **Show VNext** at the bottom to get guidance

**Add Tab:** **Long Touch** add a new Tab. **One Touch** toggles the visibility of File Tab Strip in the bottom. Displays number of Tabs opened.

**Disable VNext on Touch :** VNext guidance can be popped up by touching any word in editor area. This disables.

**Disable Verilog Review :** SELF ASSESSING MODE. **STOP Verilog** compilation. There will not be any syntax errors shown. Can be enabled again.

**Show VNext:** Show what to do after the currently typed, at any point of time while coding. VNext is automatically displayed to Continuously guide. **Auto VNext** Can be switched off, with a **Long Touch** or from the menu as shown above.

**Show VGyan:** Show all about the currently typed, at any point of time while coding. VGyan is not shown automatically while coding. In KeyWord mode VGyan is shown automatically.

**Keyword mode:** Key Word mode is useful to improve the understanding of all key words and operators of Verilog. There will not be any Syntax Error check, so user can type randomly any keyword or operator to understand the significance better.